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LETTERS

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Steep-slope hysteresis-free negative capacitance MoS_2 transistors

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The so-called Boltzmann tyranny defines the fundamental thermionic limit of the subthreshold slope of a metal–oxide–semiconductor field-effect transistor (MOSFET) at 60 mV dec^{-1} at room temperature and therefore precludes lowering of the supply voltage and overall power consumption[1,2]. Adding a ferroelectric negative capacitor to the gate stack of a MOSFET may offer a promising solution to bypassing this fundamental barrier[3]. Meanwhile, two-dimensional semiconductors such as atomically thin transition-metal dichalcogenides, due to their low dielectric constant and ease of integration into a junctionless transistor topology, offer enhanced electrostatic control of the channel[4–12]. Here, we combine these two advantages and demonstrate a molybdenum disulfide (MoS_2) two-dimensional steep-slope transistor with a ferroelectric hafnium zirconium oxide layer in the gate dielectric stack. This device exhibits excellent performance in both on and off states, with a maximum drain current of 510 μA μm^{-1} and a sub-thermionic subthreshold slope, and is essentially hysteresis-free. Negative differential resistance was observed at room temperature in the MoS_2 negative-capacitance FETs as the result of negative capacitance due to the negative drain-induced barrier lowering. A high on-current-induced self-heating effect was also observed and studied.

Transition-metal dichalcogenides (TMDs) have been extensively explored as two-dimensional (2D) semiconductors for future device technologies. Atomically thin MoS_2 has been widely studied as a highly promising channel material because it offers ideal electrostatic control of the channel, ambient stability, an appropriate direct bandgap and moderate mobility. The TMD is generally configured in a junctionless (JL) form, with metal–semiconductor contacts replacing the source–drain p–n junctions of a bulk transistor. JL MoS_2 field-effect transistors (FETs) exhibit high on/off ratios and strong immunity to short channel effects for transistor applications with channel length L_{ch} down to sub-5 nm (refs. [4–12]). However, the power dissipation issue remains unresolved, similar to the situation for silicon-based metal–oxide–semiconductor FET (MOSFET) scaling. To overcome the thermionic limit, several novel device concepts have been proposed that have potential subthreshold slopes (SS) less than 60 mV dec^{-1} at room temperature, including impact-ionization FETs (II-FET)[13], tunnelling FETs (T-FET)[14,15], nanoelectromechanical FETs (NEMFET)[16] and negative-capacitance (NC) FETs[17–28]. In a NC-FET, the insulating ferroelectric layer serves as a negative capacitor so that the channel surface potential can be amplified more than the gate voltage, and hence the device can operate with SS less than 60 mV dec^{-1} at room temperature[3]. The simultaneous fulfilment of internal gain and the non-hysteretic condition is crucial to the proper design of capacitance matching in a stable NC-FET. Meanwhile, channel transport in NC-FETs remains unperturbed. Therefore, coupled with the flatness of the body capacitance of TMD materials and symmetrical operation around the zero-charge point in a JL transistor, performance in 2D JL-NC-FETs is expected to improve for both on and off states. Accordingly, it would be highly desirable to integrate a ferroelectric insulator and 2D ultrathin channel materials to create a 2D JL-NC-FET to achieve high on-state performance for high operating speed and sub-thermionic SS for low power dissipation.

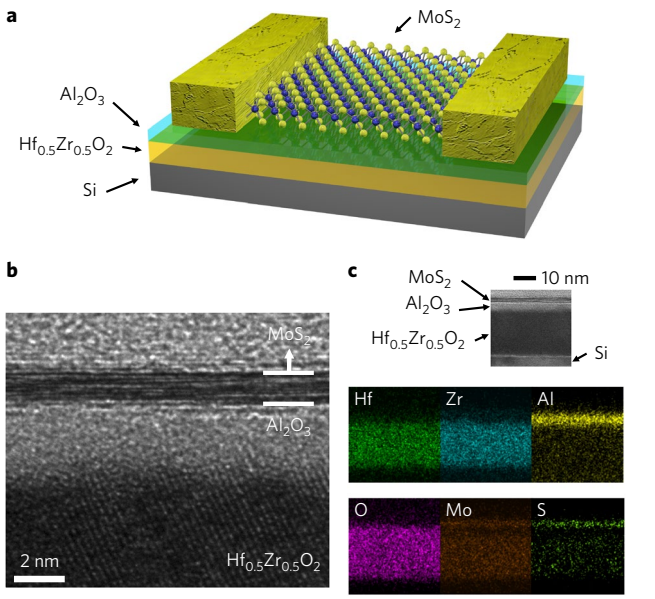

Fig. 1 | Schematic and fabrication of MoS_2 NC-FETs. a, Schematic view of a MoS_2 NC-FET. The gate stack includes heavily doped Si as the gate electrode, 20 nm HZO as the ferroelectric capacitor, 2 nm Al_2O_3 as the capping layer and capacitance-matching layer. A 100 nm Ni layer was deposited using an electron-beam evaporator as the source–drain electrode. **b**, Cross-sectional view of a representative sample showing the bilayer MoS_2 channel, amorphous Al_2O_3 and polycrystalline HZO gate dielectric. **c**, Corresponding EDS elemental map showing the distribution of Hf, Zr, Al, O, Mo and S.

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Here, we demonstrate steep-slope MoS_2 NC-FETs by introducing ferroelectric hafnium zirconium oxide (HZO) into the gate stack. These transistors exhibit essentially hysteresis-free switching characteristics with a maximum drain current of 510 μA μm^{-1} and sub-thermionic SS. The maximum drain current of the NC-FETs fabricated in this work was found to be around five times larger than in MoS_2 FETs fabricated on 90 nm SiO_2 using the same process. As will be discussed in the following, this is a direct consequence of on-state current enhancement in a JL-NC-FET. Negative differential resistance (NDR), correlated to the negative drain-induced barrier lowering (DIBL) at the off state, is observed because of the drain-coupled negative capacitance effect. Remarkably, the high performance is sustained despite significant self-heating in the transistors, in contrast to traditional bulk MOSFETs.

The MoS_2 NC-FET shown in Fig. 1a consists of a monolayer to a dozen layers of MoS_2 as the channel, a 2 nm amorphous aluminium oxide (Al_2O_3) layer and a 20 nm polycrystalline HZO layer as the gate dielectric, heavily doped silicon substrate as the gate electrode and nickel source–drain contacts. HZO was chosen for its ferroelectricity, its CMOS-compatible manufacturing, and the ability to scale down its equivalent oxide thickness (EOT) to ultrathin dimensions[23–28]. The amorphous Al_2O_3 layer was applied for capacitance matching and gate leakage current reduction through the polycrystalline HZO. A cross-sectional transmission electron microscopy (TEM)

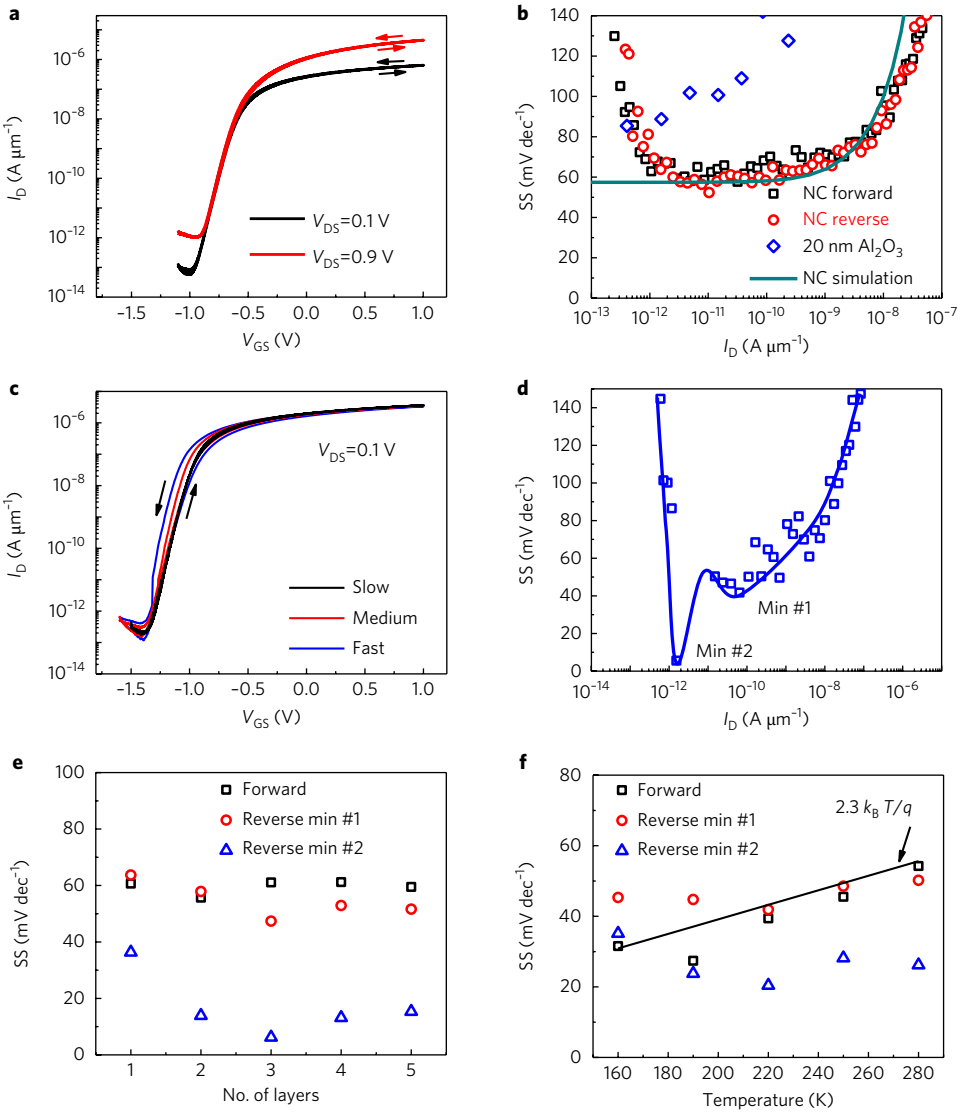

Fig. 2 | Off-state switching characteristics of MoS_2 NC-FETs. a, I_D–V_{GS} characteristics measured at room temperature and at V_{DS} = 0.1 V and 0.9 V. V_{GS} step is 0.5 mV. The thickness of the MoS_2 flake is 8.6 nm, measured by AFM. The device has a channel length of 2 μm and channel width of 3.2 μm, and RTA was performed at 500 °C during substrate preparation. **b**, SS versus I_D characteristics of the device in **a**, showing minimum SS below 60 mV dec^{-1} for both forward and reverse sweeps. Also shown is a comparison of SS versus I_D characteristics with simulation results on the same device structure and an experimental MoS_2 FET with 20 nm Al_2O_3 only as gate oxide. **c**, I_D–V_{GS} characteristics measured at room temperature and at V_{DS} = 0.1 V at different gate voltage sweep speeds. V_{GS} steps were set to be from 0.3 to 5 mV. The thickness of the MoS_2 flake is 5.1 nm. This device has a channel length of 1 μm and channel width of 1.56 μm. The RTA temperature was 400 °C for the gate dielectric. **d**, SS versus I_D characteristics during fast reverse sweep of the device in **c**. The SS versus I_D characteristics show two local minima (min #1 and min #2). min #2 suggests switching between different polarization states of the ferroelectric HZO. **e**, Layer dependence of SS for one to five layers. The SS of the MoS_2 NC-FETs shows weak thickness dependence. **f**, Temperature dependence of SS from 160 K to 280 K. The measured SS is below the thermionic limit down to 220 K. SS below 190 K is above the thermionic limit because of the stronger impact of the Schottky barrier on SS.

image of a representative MoS_2 NC-FET is shown in Fig. 1b, and a detailed energy-dispersive X-ray spectrometry (EDS) elemental map is presented in Fig. 1c. The EDS analysis confirmed the presence and uniform distribution of elements Hf, Zr, Al, O, Mo and S. No obvious interdiffusion of Hf, Zr and Al was found. The gate stack was assessed for its rapid thermal annealing (RTA) temperature dependence with a metal–oxide–semiconductor capacitor structure by carrying out fast I–V measurements. Measured hysteresis loops for polarization versus electric field (P–E) as well as X-ray diffraction (XRD) results suggest that RTA at 400–500 °C after atomic layer deposition (ALD) enhances the ferroelectricity (Supplementary Section 1).

The electrical characteristics of MoS_2 NC-FETs are strongly dependent on the ferroelectricity of the HZO layer, which is defined by the film annealing temperature and gate–source voltage (V_{GS}) sweep speed. In addition to standard I–V measurements, hysteresis was measured as the difference in V_{GS} in forward (from low to high) and reverse (from high to low) V_{GS} sweeps at $I_D = 1\,nA\,\mu m^{-1}$ and $V_{DS} = 0.1\,V$. Here, we study the room-temperature characteristics of MoS_2 NC-FETs. Figure 2a presents the I_D–V_{GS} characteristics of a device with the gate dielectric annealed at 500 °C, measured in V_{GS} steps of 0.5 mV. This device has a channel length of 2 µm, channel width of 3.2 µm and channel thickness of 8.6 nm. The hysteresis (~12 mV) is small and essentially negligible, consistent with theory for the NC-FET, and the gate leakage current I_G is negligible (Supplementary Section 2). Figure 2b presents SS vs I_D data for the device examined in Fig. 2a, as well as a comparison of the simulation results and experimental results with only 20 nm Al_2O_3 as the gate dielectric. MoS_2 FETs fabricated on a 20 nm Al_2O_3 conventional dielectric present a typical SS of 80–90 mV dec^{-1}, much larger than the values for NC-FETs. The SS was extracted for both forward sweep (SS_{For}) and reverse sweep (SS_{Rev}), and the device was observed to exhibit $SS_{Rev} = 52.3\,mV\,dec^{-1}$ and $SS_{For} = 57.6\,mV\,dec^{-1}$. SS values below 60 mV dec^{-1} at room temperature are thus conclusively demonstrated for both forward and reverse sweeps in this near hysteresis-free device.

Because the HZO polarization depends on the sweep rate, electrical characterization of the MoS_2 NC-FETs was also carried out at different V_{GS} sweep speeds. This speed was controlled by modifying the V_{GS} measurement step from 0.3 mV to 5 mV. Figure 2c presents I_D–V_{GS} characteristics for a few-layer MoS_2 NC-FET measured at slow, medium and fast sweep speeds, corresponding to V_{GS} steps of 0.3, 1 and 5 mV. Hysteresis of the MoS_2 NC-FETs was found to be diminished by reducing the sweep speed. A plateau and a minimum characterize the SS vs I_D plot during the reverse sweep. These features ($SS_{Rev,min\#1}$ and $SS_{Rev,min\#2}$) were observed in almost all the fabricated devices when measured with fast sweep V_{GS}, as shown in Fig. 2d. The second local minimum of SS is the result of switching between two polarization states of the ferroelectric oxide, which is associated with loss of capacitance matching at high speed. When measured in fast sweep mode with a V_{GS} step of 5 mV, the device exhibits $SS_{For} = 59.6\,mV\,dec^{-1}$, $SS_{Rev,min\#1} = 41.7\,mV\,dec^{-1}$ and $SS_{Rev,min\#2} = 5.6\,mV\,dec^{-1}$. Overall, the average SS is less than 60 mV dec^{-1} for over four decades of drain current. In slow sweep

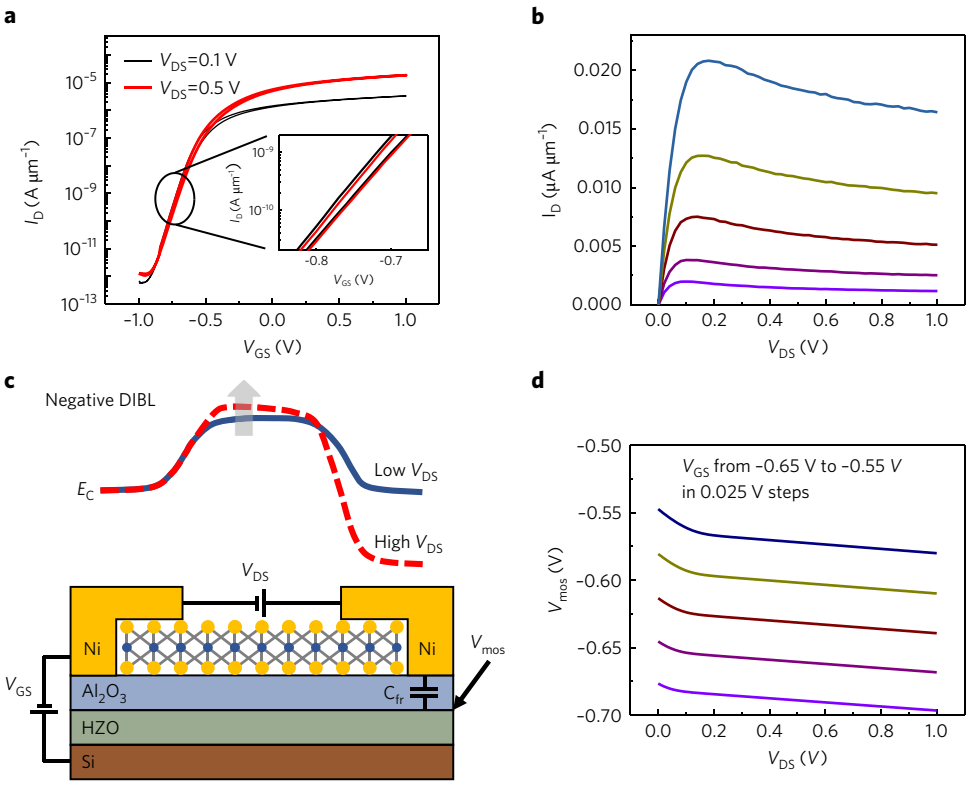

Fig. 3 | NDR and negative DIBL in MoS_2 NC-FETs. a, I_D–V_{GS} characteristics measured at room temperature and at $V_{DS} = 0.1$ V and 0.5 V. The V_{GS} step during measurement was 5 mV. Inset: Zoom-in of the I_D–V_{GS} curve between −0.8 and −0.7 V. A threshold voltage shift towards the positive can be observed at high V_{DS}, indicating a negative DIBL effect. The thickness of the MoS_2 flake is 5.3 nm, estimated from AFM characterization. This device has a channel length of 2 µm and channel width 5.6 µm. A 500 °C RTA procedure in N_2 was performed for 1 min during preparation of the gate dielectric. **b**, I_D–V_{DS} characteristics measured at room temperature at V_{GS} from −0.65 to −0.55 V in 0.025 V steps. Clear NDR can be observed because of the negative DIBL effect induced by negative capacitance. **c**, Band diagram of the negative DIBL effect. The negative DIBL origins from capacitance coupling from the drain to the interfacial layer between Al_2O_3 and HZO. **d**, Simulation of interfacial potential vs V_{DS}. When V_{DS} is increased, the interfacial potential is reduced, and the carrier density in the MoS_2 channel is reduced. Thus, the channel resistance is increased and drain current is reduced.

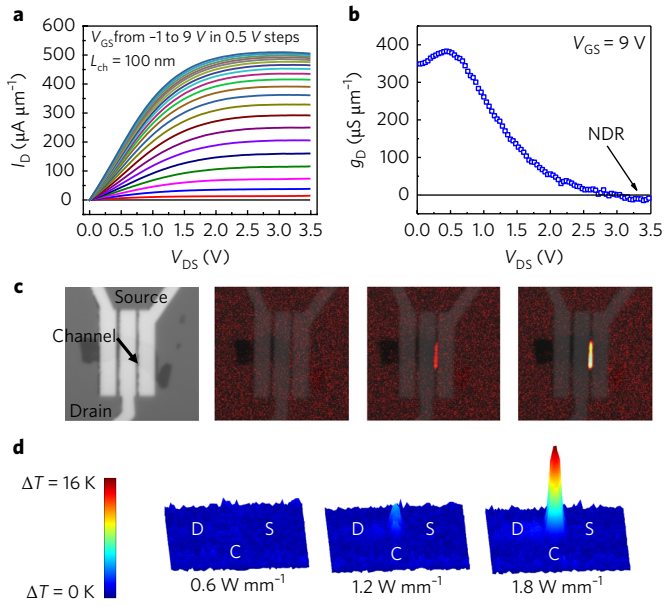

Fig. 4 | On-state characteristics and self-heating of MoS_2 NC-FETs. **a**, I_D–V_{DS} characteristics measured at room temperature at V_{GS} from −1 V to 9 V in 0.5 V steps. The thickness of the MoS_2 flake is 3 nm. This device has a channel length of 100 nm. The maximum stress voltage/EOT in this device is about 2 V nm^{-1}. Maximum drain current is 510 μA μm^{-1}. Clear negative drain differential resistance can be observed at high V_{GS}. **b**, g_D–V_{DS} characteristics for the device in **a** at V_{GS} = 9 V. g_D less than zero at high V_{DS} highlights the NDR effect due to self-heating. **c**,**d**, Thermoreflectance images (**c**) and temperature maps (**d**) at power densities from 0.6 W mm^{-1} to 1.8 W mm^{-1}. The heated channel suggests that the self-heating effect has to be taken into account in MoS_2 NC-FETs with large drain current.

mode, no obvious second local minimum and hysteresis can be observed, as shown in Fig. 2a, reflecting well-matched capacitances throughout the subthreshold region. Figure 2e shows the thickness dependence of SS from a monolayer to five layers of MoS_2 for the channel (see Supplementary Section 4 for determination of layer number). No obvious thickness dependence is observed. Figure 2f shows the temperature dependence of SS for a MoS_2 NC-FET measured from 280 K to 160 K. The measured SS is below the thermionic limit down to 220 K. SS below 190 K is above the thermionic limit because of the stronger impact of the Schottky barrier at lower temperatures. Detailed I–V characteristics at low temperature are provided in Supplementary Section 5.

Although the above MoS_2 NC-FET shows an average SS during reverse sweep of <60 mV dec^{-1} for more than four decades, low hysteresis is generally required for any transistor application. A detailed discussion of the non-hysteretic and internal gain conditions of the MoS_2 NC-FET is provided in Supplementary Section 7 using experimentally measured P–E results taken directly on HZO films. We found that both SS and hysteresis in MoS_2 NC-FETs are sensitive to the annealing temperature for the gate dielectric. The dependence of SS on different RTA temperatures was studied systematically (Supplementary Section 3), and it was found that MoS_2 NC-FETs with RTA at 400 °C and 500 °C have smaller SS values than as-grown samples and 600 °C annealed samples, as shown in Supplementary Fig. 4. This conclusion can also be obtained from the hysteresis loop of plots of P–E, because the gate stacks with RTA at 400 °C and 500 °C show larger remnant polarization, indicating stronger ferroelectricity. A statistical study on temperature-dependent hysteresis is provided in Supplementary Fig. 4d. It was found that MoS_2 NC-FETs with 500 °C RTA exhibit the lowest hysteresis when compared with devices without RTA and devices with RTA at 400 °C and 600 °C. Therefore, RTA temperature engineering could be useful in achieving both steep slope and low hysteresis.

DIBL is widely noted as major evidence for short-channel effects in MOSFETs[2]. In conventional MOSFETs, the threshold voltage V_{th} shifts in the negative direction, relative to the drain voltage. The DIBL, defined as $-\Delta V_{th}/\Delta V_{DS}$, is usually positive. It has been predicted theoretically that with a ferroelectric insulator introduced into the gate stack of a practical transistor, the DIBL could be reversed in NC-FETs[29]. NDR can occur naturally as a result of the negative DIBL effect. Figure 3a shows negative DIBL in the I_D–V_{GS} characteristics of another device with a channel length of 2 μm, channel width of 5.6 μm, channel thickness of 7.1 nm, and with 2 nm Al_2O_3 and 20 nm HZO as the gate dielectric. It is evident that the I_D–V_{GS} curve shifts positively when V_{DS} increases from 0.1 to 0.5 V. As this negative DIBL occurs around the off state, NDR is also observed simultaneously in the same device in the off state, as shown in Fig. 3b. Figure 3c presents the band diagram for the negative DIBL effect. This negative DIBL originates from capacitance coupling from the drain to the interfacial layer between Al_2O_3 and HZO. The interfacial layer potential V_{mos} can be estimated as a constant when the thickness of the ferroelectric oxide layer is thin (Supplementary Section 7). Simulation of V_{mos} shows that, when V_{DS} is increased, the interfacial potential is reduced (Fig. 3d), indicating that the carrier density in the MoS_2 channel is reduced. Thus, the channel resistance is increased, leading to the NDR effect.

The EOT of the gate stack (2 nm Al_2O_3 and 20 nm HZO) in this work was measured to be 4.4 nm by C–V measurements. The breakdown voltage was consistently measured to be ~11 V. Breakdown voltage/EOT was 2.5 V nm^{-1}, which is about 2.5 times larger than the value for SiO_2. It can be verified easily that breakdown voltage/EOT is proportional to the electric displacement field. As it is well known from Maxwell's equations that the electric displacement field is proportional to charge density, higher breakdown voltage/EOT could lead to a higher carrier density. Figure 4a presents the I_D–V_{DS} characteristics (measured at room temperature) of a MoS_2 NC-FET with 100 nm channel length. The thickness of the MoS_2 flake is 3 nm. The gate voltage was stressed up to 9 V and the maximum gate voltage/EOT in the device was ~2 V nm^{-1}. A maximum drain current of 510 μA μm^{-1} was achieved, which is about five times larger than in control devices using 90 nm SiO_2 as the gate dielectric. Note that this maximum drain current was obtained without special contact engineering such as doping[11] or using a heterostructure contact stack[10]; indeed, as discussed in the Supplementary Section 7, the JL topology is key to improving the performance of the transistor. This is an important but unexplored advantage of using a ferroelectric gate stack to enhance on-state performance. Another type of NDR (Fig. 4b) is also clearly observed when the device is biased at high V_{GS} because of the self-heating effect from large drain current and voltage. Figure 4c presents thermo-reflectance images taken at power densities from 0.6 W mm^{-1} to 1.8 W mm^{-1}. The heated channel, with its temperature increased to ~40 °C, suggests the self-heating effect. This potentially degrades channel mobility and limits the maximum drain current, and thus has to be taken into account in MoS_2 NC-FETs.

In conclusion, we have successfully demonstrated MoS_2 2D NC-FETs with promising on- and off-state characteristics. The stable, non-hysteretic and bidirectional sub-thermionic switching characteristics have been unambiguously confirmed to be the result of a NC effect. On-state performance is enhanced, with a maximum drain current of 510 μA μm^{-1} at room temperature, which leads to the self-heating effect. Finally, we have shown that the observed NDR is induced by the negative DIBL effect. After submission and during revision of this manuscript, the authors became aware of a related work being published[30].

Methods

Methods, including statements of data availability and any associated accession codes and references, are available at https://doi.org/10.1038/s41565-017-0010-1.

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Author contributions

P.D.Y. conceived the idea and supervised the experiments. C.J.S. performed the ALD of HZO and Al_2O_3 and dielectric physical analysis. M.S. performed the device fabrication, d.c. and *C–V* measurements, and data analysis. M.S. and N.J.C. carried out the fast *I–V* measurement. M.S. and G.Q. performed the AFM measurement. H.Z., K.D.M. and A.S. did the thermo-reflectance imaging. G.Q. performed the Raman and photoluminescence experiment. C.T.W. conducted TEM and EDS analyses. C.J. and A.M.A. conducted the theoretical calculations and analysis. M.S., A.M.A. and P.D.Y. summarized the manuscript and all authors commented on it.

Competing financial interests

The authors declare no competing financial interests.

Additional information

Supplementary information is available for this paper at https://doi.org/10.1038/s41565-017-0010-1.

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Methods

ALD deposition. $Hf_{1-x}Zr_xO_2$ film was deposited on a heavily doped silicon substrate. Before deposition, the substrate was cleaned by RCA standard cleaning and a diluted HF dip to remove organic and metallic contaminants, particles and unintentional oxides, followed by a deionized water rinse and drying. The substrate was then transferred to an ALD chamber to deposit $Hf_{1-x}Zr_xO_2$ film at 250 °C, using $[(CH_3)_2N]_4Hf$ (TDMAHf), $[(CH_3)_2N]_4Zr$ (TDMAZr) and H_2O as the Hf precursor, Zr precursor and oxygen source, respectively. The $Hf_{1-x}Zr_xO_2$ film ($x = 0.5$) was achieved by controlling the HfO_2:ZrO_2 cycle ratio of 1:1. To encapsulate the $Hf_{1-x}Zr_xO_2$ film, an Al_2O_3 layer was in situ deposited using $Al(CH_3)_3$ (TMA) and H_2O, also at 250 °C.

Device fabrication. A 20 nm $Hf_{0.5}Zr_{0.5}O_2$ layer was deposited by ALD as a ferroelectric insulator layer on the heavily doped silicon substrate after standard surface cleaning. Another 10 nm aluminium oxide layer was deposited as an encapsulation layer to prevent the degradation of HZO by reaction with moisture in the air. A BCl_3/Ar dry etching process was carried out to adjust the thickness of the Al_2O_3 down to 2 nm for capacitance matching. The rapid thermal annealing process was then performed in nitrogen ambient for 1 min at various temperatures. MoS_2 flakes were transferred to the substrate by scotch tape-based mechanical exfoliation. Electrical contacts formed from a 100 nm nickel electrode were fabricated using electron-beam lithography, electron-beam evaporation and a lift-off process.

Device characterization. The thickness of the MoS_2 was measured using a Veeco Dimension 3100 atomic force microscope (AFM) system. Electrical (d.c.) characterization was carried out with a Keysight B1500 system. Fast I–V measurements were performed using a Keysight B1530A fast measurement unit, and C–V measurements with an Agilent E4980A LCR meter. Room-temperature electrical data were collected with a Cascade Summit probe station and low-temperature electrical data were collected with a Lakeshore TTP4 probe station. Thermoreflectance imaging was done with a Microsanj thermoreflectance image analyser. Raman and photoluminescence measurements were carried out on a HORIBA LabRAM HR800 Raman spectrometer.

Data availability. The data that support the findings of the study are available from the corresponding author upon reasonable request.

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SUPPLEMENTARY INFORMATION

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Steep-slope hysteresis-free negative capacitance MoS_2 transistors

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Supplementary Information for:

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1. Fast I-V measurement of ferroelectric MOS capacitors

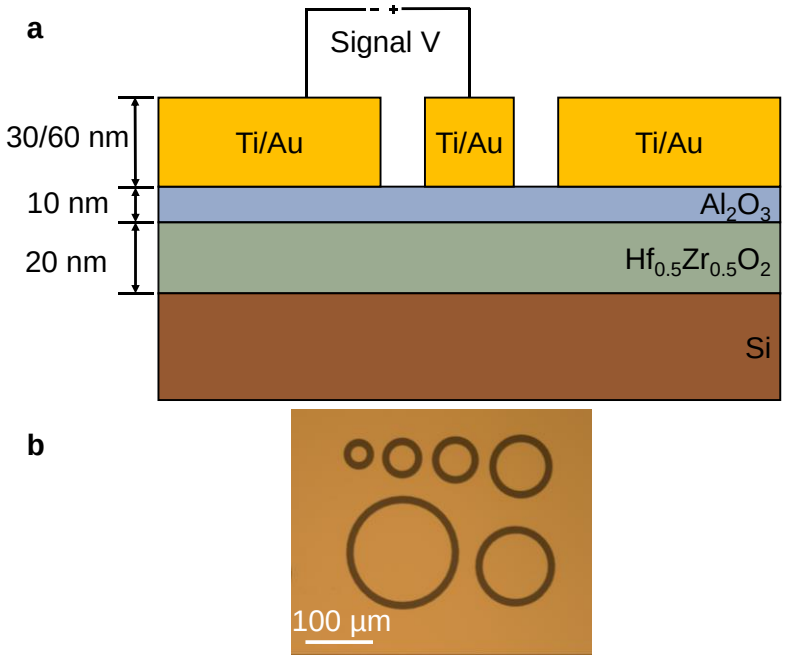

Figure S1 | Illustration of MOS structure for Pulsed I-V measurement. a Schematic diagram of a ferroelectric MOS capacitor for fast I-V measurement**. b** Optical image of the ferroelectric MOS capacitors from top view.

To study ferroelectric characteristics of the gate stack, a ferroelectric test structure is designed for fast I-V and C-V measurement. Fig. S1a shows the schematic of the ferroelectric MOS capacitor for test structure and Fig. S1b shows an optical image of the ferroelectric MOS capacitors. Hafnium zirconium oxide (HZO) was deposited by atomic layer deposition (ALD) for 20 nm as ferroelectric insulator layer on heavily doped silicon substrates. Another 10 nm aluminum oxide (Al_2O_3) layer was deposited as an encapsulation layer for capacitance matching and to prevent degradation of HZO due to air exposure. The annealing process was performed in rapid thermal annealing (RTA) in nitrogen ambient for 1 minute at various temperatures. Ti/Au with 30 nm/60 nm was used as electrode metal.

To validate the ferroelectricity of the gate stack used in this work, current response to a triangular voltage signal was measured to characterize the hysteresis loop of polarization versus electric field (P-E). All current responses from no RTA to 600 ^{o}C RTA deviate from a square wave signal, indicating the MOS capacitors measured in this work is not linear capacitors (Fig. S2a). The hysteresis loops of P-E at different temperatures are obtained from the integration of current response as a function of voltage, to obtain the polarized charge density[1]. From the hysteresis loop of P-E, it is confirmed that the samples with 400 ^{o}C and 500 ^{o}C exhibit stronger ferroelectricity, compared to those with no RTA or 600 ^{o}C.

Grazing incidence X-ray diffraction (GI-XRD) analysis in Fig. S2d depicts the crystallization behaviors of HZO with no RTA and 400 ^{o}C. The sample with 400 ^{o}C reveals apparent orthorhombic phases (o-phases). The formation of non-centrosymmetric o-phase is believed to lead to the ferroelectricity of HZO films after annealing[2,3], as confirmed in Fig. S2b. The slightly crystallized HZO found in the sample with no RTA is attributed to the thermal budget of ALD Al_2O_3 deposition.

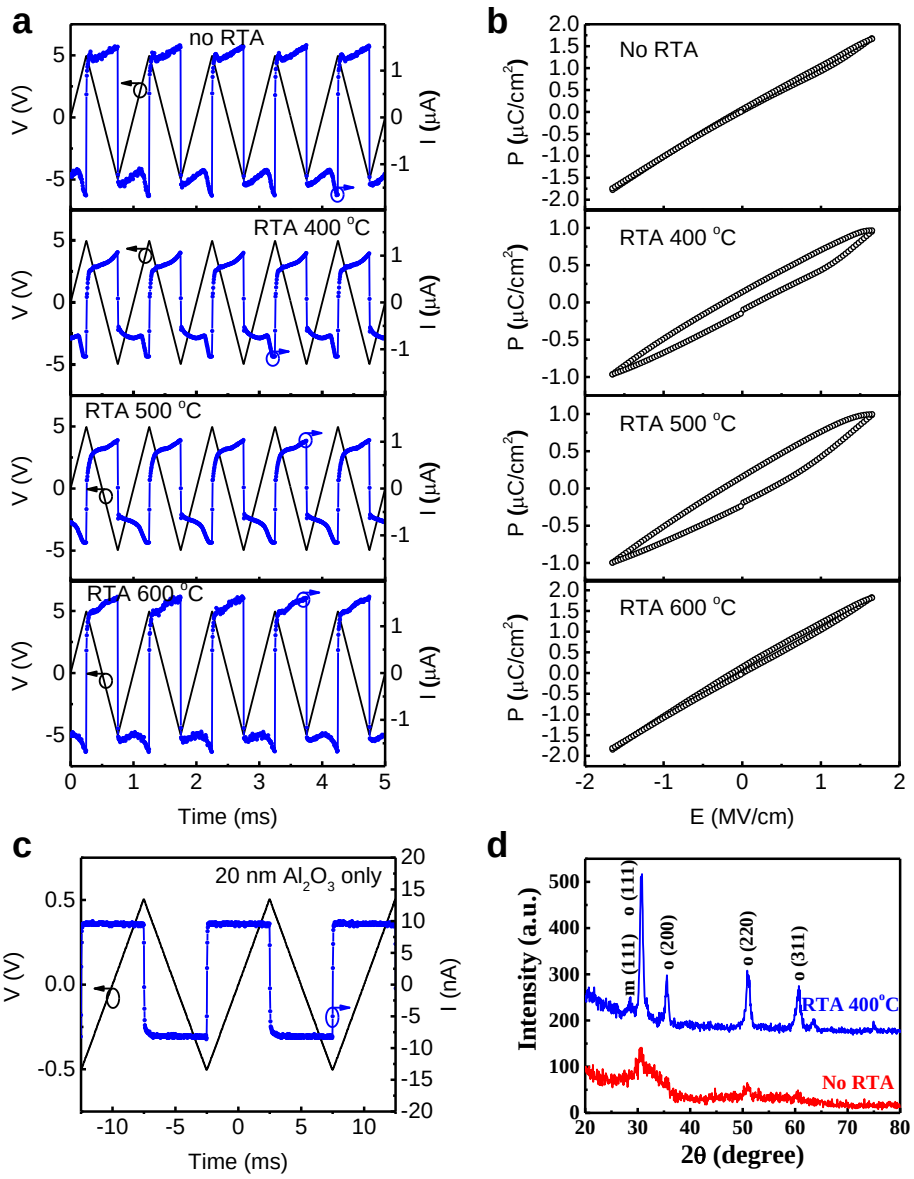

Figure S2 | Ferroelectricity in the gate stack. a Current response to a triangular voltage signal of the ferroelectric capacitor in Fig. S1 without RTA and with RTA from 400 °C to 600 °C in N_2 ambient for 1 min. **b** Temperature dependence of the P-E hysteresis curves obtained from a. **c** Current response of a linear capacitor with 20 nm Al_2O_3 only as dielectric. **d** GI-XRD diffractograms of HZO. The formation of non-centrosymmetric o-phase is believed to lead to the ferroelectricity of HZO films after annealing at 400°C.

2. Gate leakage current of MoS_2 NC-FETs

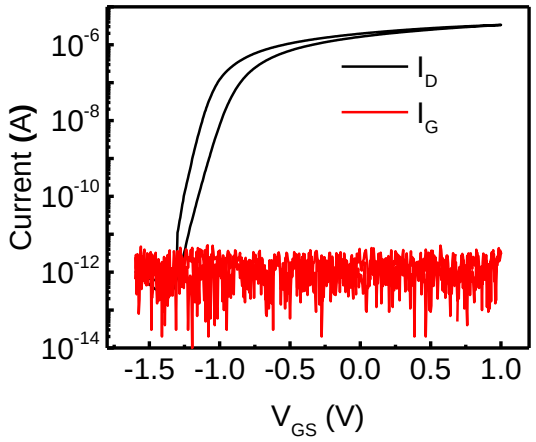

Figure S3 | Gate leakage current in MoS_2 NC-FETs. Gate leakage current and I_D-V_{GS} characteristics simultaneously measured in the MoS_2 NC-FET for Fig. 2c.

The gate leakage current was measurement simultaneously with I_D, as shown in Fig. S3. It is the gate leakage current and I_D-V_{GS} characteristics simultaneously measured in the MoS_2 NC-FET for Fig. 2c. A constant gate leakage current ~pA level means the gate leakage current is negligible in subthreshold region and the measured leakage is the lower detection limit of the equipment, as a medium power SMU is used for gate leakage current to speed up measurement here instead of a high-resolution SMU for I_D.

3. Effect of RTA temperature on the subthreshold slope of MoS_2 NC-FETs

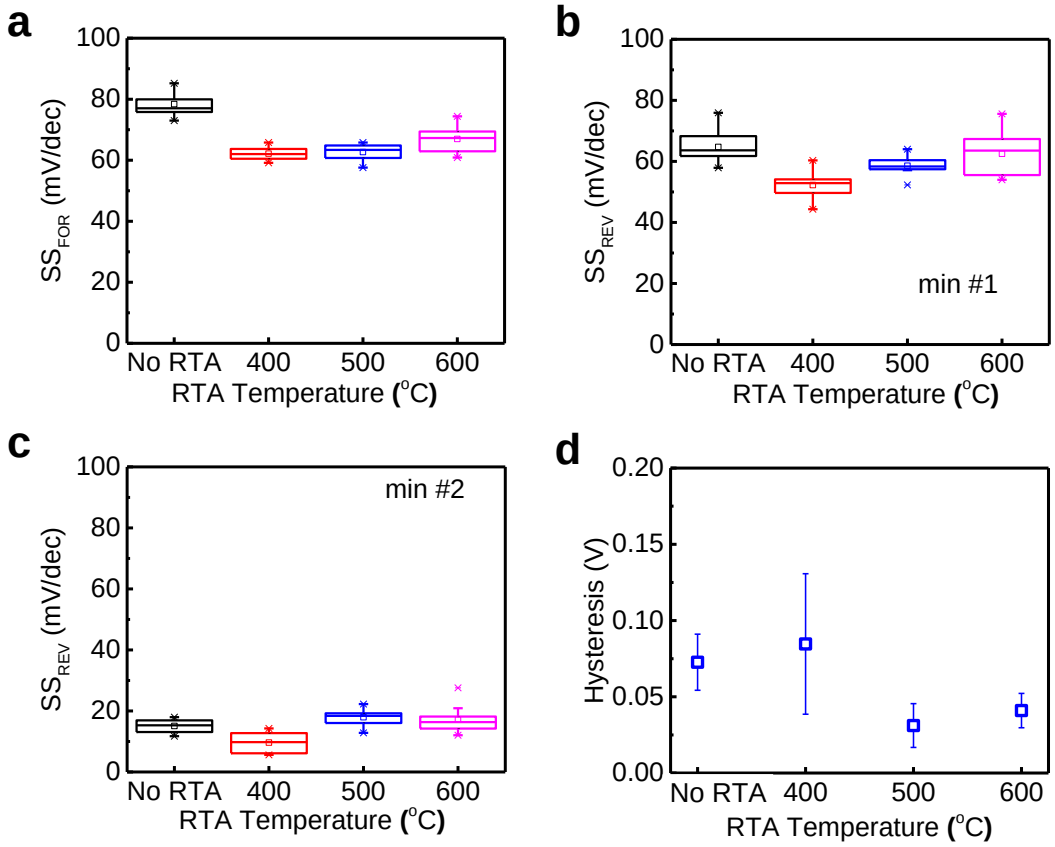

Figure S4 | Statistic study of the effect of RTA temperature on the subthreshold slope and hysteresis of MoS_2 NC-FETs. a SS_{For}, **b** $SS_{Rev,min\#1}$, **c** $SS_{Rev,min\#1}$. **d** hysteresis. Each data point contains the measurement of at least 8 individual devices with the same fabrication process. The SS and hysteresis presented here are all from I_D-V_{GS} characteristics measured at 5 mV V_{GS} step. The hysteresis is measured as V_{GS}-difference between forward and reverse sweeps at I_D=1 nA/μm and at V_{DS}=0.1 V. All the devices have the device structure as shown in Fig. 1.

As the annealing temperature is quite critical to ferroelectricity of the gate stack, we carried out the statistic study of the effect of RTA temperature on the SS of MoS_2 NC-FETs. As the RTA was performed after the gate stack deposition and before the transfer of MoS_2 flake, only the substrate, HZO and Al_2O_3 were affected. Fig. S4a-c shows the SS_{For}, $SS_{Rev,min\#1}$ and $SS_{Rev,min\#2}$ versus RTA temperature, respectively. It is found that devices with 400 °C RTA show the lowest

SS for all three SS characteristics. Meanwhile, devices with 500 ^{o}C RTA have lower SS_{For} and $SS_{Rev,min\#1}$ than devices without RTA and devices with 600 ^{o}C RTA. This RTA temperature dependence of SS is very consistent with the results from Fig. S2. Devices with 400 ^{o}C or 500 ^{o}C RTA have lower SS comparing with devices without RTA or with 600 ^{o}C RTA because the stronger ferroelectricity, as shown in Fig. S2b. A statistic study on temperature dependent hysteresis is shown in Fig. S4d. It is found that MoS_2 NC-FETs with 500 ^{o}C RTA exhibit the lowest hysteresis comparing with devices without RTA, devices with RTA at 400 ^{o}C and 600 ^{o}C. All hysteresis data collected here is from I_D-V_{GS} characteristics measured in fast sweep mode with 5 mV V_{GS} step and at V_{DS}=0.1 V.

4. Layer number determination of MoS_2 flake and mono-layer MoS_2 NC-FET

Monolayer, bi-layer and multi-layer MoS_2 flakes were identified using three techniques: Raman shift[4], photoluminescence spectra[5] and AFM measurement[6]. There are two characteristic Raman modes, the in-plane vibrational mode and the out-of-plane vibrational mode with $\Delta\omega$=18.5 cm^{-1} indicating mono-layer and $\Delta\omega$=21.4 cm^{-1} indicating bi-layer, as shown in Fig. S5a. Meanwhile, mono-layer MoS_2 is well known to have a direct bandgap so that there is a strong peak in photoluminescence spectra as shown in Fig. S5b. It is straight forward to distinguish mono-layer MoS_2 from bi-layer or few-layer MoS_2. AFM measurement is also applied to determine the thickness and a mono-layer MoS_2 flake in this work is measured to be around 0.9 nm, as shown in Fig. S5c. Fig. S5d shows the I_D-V_{GS} characteristics of a mono-layer MoS_2 NC-FET. Severe SS degradation is observed at low V_{DS} due to the large Schottky barrier height for mono-layer MoS_2 at metal/channel contacts.

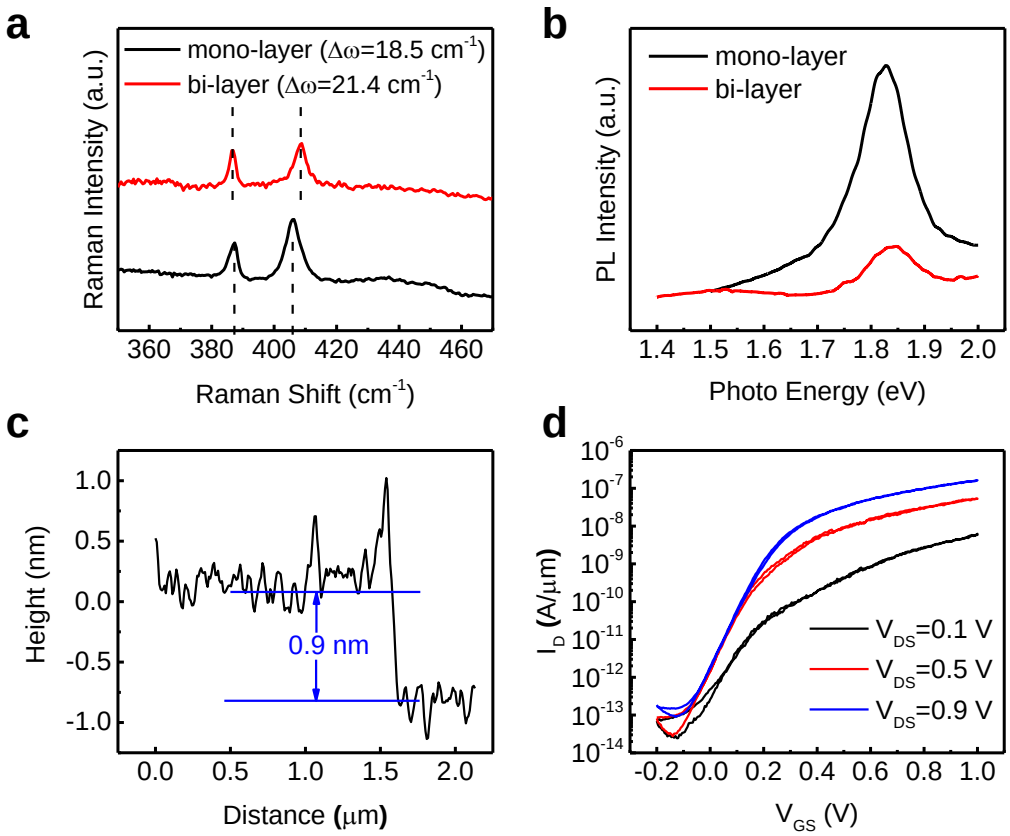

Figure S5 | Mono-layer identification and monolayer MoS_2 NC-FET. a Raman spectrum measurement of mono-layer and bi-layer MoS_2. **b** Photoluminescence measurement of single-layer and bi-layer MoS_2. **c** AFM measurement of a mono-layer MoS_2 flake. **d** I_D-V_{GS} characteristics of a mono-layer MoS_2 NC-FET with 0.5 μm channel length.

5. Low temperature measurement of a bi-layer MoS_2 NC-FET

Fig. S6 shows the low temperature measurement of a bi-layer MoS_2 NC-FET from 160 K to 220 K. The device has a channel length of 0.5 μm and a channel width of 2.5 μm. The low temperature electrical data was collected with a Lakeshore TTP4 probe station. Measured SS is below the thermionic limit down to 220 K. SS below 190 K shows above the thermionic limit because of stronger impact of Schottky barrier on SS.

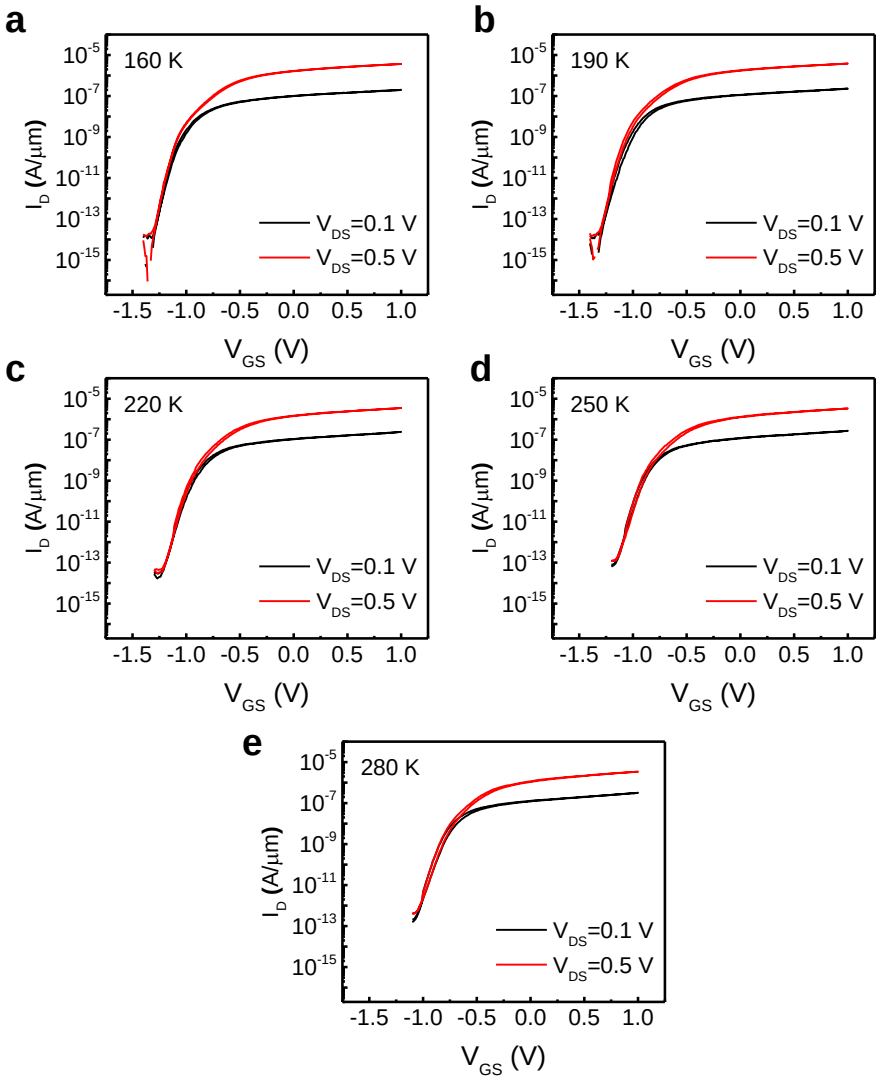

Figure S6 | Low temperature measurement of a bi-layer MoS_2 NC-FET. I_D-V_{GS} characteristics of a bi-layer MoS_2 NC-FET with 0.5 μm channel length, 2.5 μm channel width. **a** 160 K. **b** 190 K. **c** 220 K. **d** 250 K. **e** 280 K.

6. Experiment setup for thermoreflectance imaging

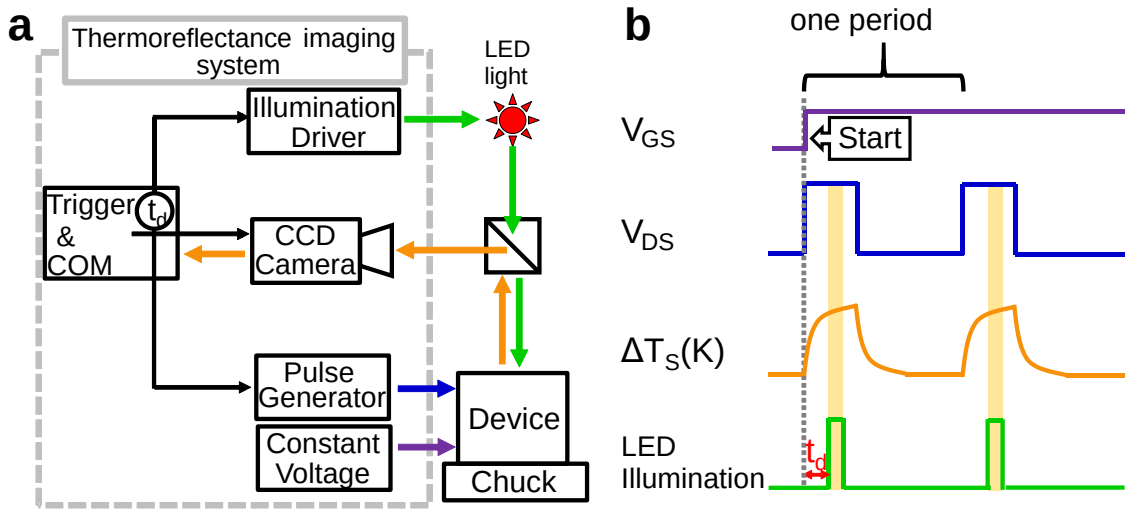

Figure S7 | Illustration of thermoreflectance imaging measurement system. a A schematic of thermoreflectance imaging system. A pulse generator (V_{DS}) and a constant voltage source (V_{GS}) drive the transistor. A control computer triggers the illumination driver and the CCD camera for a given delay time with respect to V_{DS}. **b** Timing diagram for transient TR imaging with a given LED delay time (t_d).

The thermoreflectance (TR) measurement system setup is shown in Fig. S7[7,8]. A high-speed LED pulse illuminates the device, and a synchronized chare coupled device (CCD) camera captures the reflected image, as shown in Fig. 7a. The MoS_2 is illuminated through an LED (λ = 530 nm) via an objective lens. The reflected light from the surface of MoS_2 channel is captured on a variable frame rate, 14-bit digitization, Andor CCD camera.

For the transient measurement of temperature, the device is periodically turned ON and OFF by a V_{DS} pulse, as shown in Fig. S7b, allowing the channel to heat and cool, respectively. By controlling the delay of the LED pulse with respect to the beginning of the V_{DS} pulse, the TR image can capture different phases of the transient heating and cooling kinetics. The delay time for the LED illumination can be varied and each illumination pulse acts as a camera shutter. Every V_{DS} cycle produces an image capturing the thermal state of the substrate at a given time delay. The

average of these images improves the signal-to-noise ratio and produces a high-resolution map of temperature. In this work, temperature was measured at the last 100 μs of the 1 ms drain voltage pulse (10 ms period).

The change in reflectivity (ΔR) under visible spectral range is proportional to the change in temperature, so that once the TR coefficient is obtained, ΔR can be mapped to differential increase in temperature (ΔT_S). Unfortunately, TR coefficient must be calibrated, because it depends on the wavelength, the angle of incidence, and the polarization of the incident light, as well as the surface properties of the reflecting material. The calibration is performed by heating the sample by placing it on an external microthermoelectric stage. The temperature of the sample is monitored by micro-thermocouple while capturing the reflection changes by the CCD camera. The TR coefficient for the specific setup is obtained by plotting the change in reflectivity as a function of temperature measured by the thermocouple. Here, TR coefficient is calibrated on exfoliated MoS_2 flakes.

7. Simulation of MoS_2 NC-FETs

As shown in Fig. S8a a negative capacitance MoS_2 transistor can be treated as an intrinsic MoS_2 transistor in series with an HZO ferroelectric capacitor. In addition, the electrical behavior of HZO ferroelectric capacitor can be described by Landau-Khalatnikov (LK) equation[9-11]. Landau coefficients are extracted from the experimental P-E curve of HZO. For the intrinsic MoS_2 transistor, one can obtain its transfer characteristic and output characteristic using classical drift-diffusion method. To simulate the experimental device (metal (Heavily-doped silicon)-ferroelectric oxide-insulator-semiconductor), we will assume that the potential distribution is essentially uniform across the gate dielectric, which simplifies the overall analysis by allowing one to decouple the HZO dielectric from the standard MOSFET structure[12-14]. In fact, the errors caused by this approximation can be ignored when the thickness of ferroelectric layer is not too thick[15,16]. The other device parameters are extracted from the experimental transfer characteristics. All simulations assume 1 μm channel length, 8.6 nm thick MoS_2 flake, and 2 nm Al_2O_3 capping, unless otherwise specified.

Landau coefficients (α, β, γ) are extracted from the P-E measurement on the TiN/HZO/TiN structure, as shown in Fig. S8c, in which ALD HZO process condition is exactly same as the one for the HZO/Al_2O_3 stacks but with TiN as top and bottom metallic electrodes. The complete LK equation is written as[17],

$$V_{GS} = V_{mos} + V_f = V_{mos} + 2t_f \alpha Q_{av} + 4t_f \beta Q_{av}^3 + 6t_f \gamma Q_{av}^5 + \rho t_f \frac{dQ_{av}}{dt} \quad (1)$$

$$Q_{av} = \frac{Q_{ch}+Q_{p1}+Q_{p2}}{WL} \quad (2)$$

$$Q_{p1} = C_{fr} W_{ch} (V_{mos} - V_S) \quad (3)$$

$$Q_{p2} = C_{fr} W_{ch} (V_{mos} - V_D) \quad (4)$$

where Q_{av} is the average gate charges density per area. Q_{ch} is the intrinsic channel area charge, Q_{p1} is the parasitic charges caused by the source-gate capacitance, and Q_{p2} is the parasitic charges caused by the drain-gate capacitance. α, β, and γ are Landau coefficients, which are material dependent constants; t_f is the thickness of the ferroelectric film; and V_f is the external applied voltage across the ferroelectric layer. ρ is an equivalent damping constant of HZO.

The Landau coefficients are extracted to be α=-1.1911e8 m/F, β=4.32e9 $m^5/F/coul^2$, and γ=0 $m^9/F/coul^4$, as shown in Fig. S8c. Fig. S8d shows the simulation results based on these experimental Landau coefficients which exactly match with our experimental results. Based on the Landau coefficients extracted from experimental P-E and eqn. (1), the capacitance of ferroelectric capacitor (C_{FE}) can be calculated using experimental Landau coefficients,

$$C_{FE} = \frac{dQ_{av}}{dV_f} = \frac{1}{2\alpha t_f + 12\beta t_f Q_{av}^2 + 30\gamma t_f Q_{av}^4} \quad (5)$$

The internal gain condition and the non-hysteretic condition for MoS_2 NC-FETs are discussed based on the experimental P-E and extracted Landau coefficients. To prevent hysteretic behavior and obtain a steep SS at the same time, some design rules must be obeyed. These design principles could be derived from its small-signal capacitance circuit of a 2D NC-FET as shown in Fig. S8b. SS can be written as,

$$SS = \frac{2.3k_BT}{q} \cdot \frac{1}{\frac{\partial \phi_S}{\partial V_{gs}}} = \frac{2.3k_BT}{q}\left(1 + \frac{C_{2D}}{C_{ox}}\right) \cdot \left(1 - \frac{C_{device}}{|C_{FE}|}\right) \quad (6)$$

$$C_{device} = 2C_{fr} + \frac{C_{2D}C_{ox}}{C_{2D}+C_{ox}} \quad (7)$$

Note that C_{fr} is the parasitic capacitance. SS must satisfy the condition, $0<SS<2.3k_BT/q$, so that non-hysteretic behavior and a sub-thermionic SS (internal gain>1) could be obtained at the same time. The constraint conditions as the equations (8, 9) deduced from (6) are,

$$C_{device} < |C_{FE}| \quad (8)$$

$$|C_{FE}| < C_{eq} \quad (9)$$

$$C_{eq} = \left(1 + \frac{C_{ox}}{C_{2D}}\right) \cdot C_{device} \quad (10)$$

If no parasitic capacitance is considered as C_{fr}=0, the constraint conditions and SS become,

$$\frac{C_{2D}C_{ox}}{C_{2D}+C_{ox}} < |C_{FE}| \quad (11)$$

$$|C_{FE}| < C_{ox} \quad (12)$$

$$SS = \frac{2.3k_BT}{q}\left(1 + \frac{C_{2D}(|C_{FE}|-C_{ox})}{|C_{FE}|C_{ox}}\right) \quad (13)$$

To satisfy non-hysteretic conditions, $|C_{FE}|$ need to be greater than C_{device} (eqn. (8)), while to satisfy internal gain condition (internal gain>1, SS<2.3k_BT/q), $|C_{FE}|$ need to be less than C_{eq} (eqn. (9)). Note that C_{eq} equals to C_{ox} if C_{fr}=0. C^{-1} of $|C_{FE}|$, C_{device}, and C_{eq} are compared as shown in Fig. S8e with different t_f. It is clear to see that if t_f is greater than 72.5 nm, $|C_{FE}|$ becomes smaller than C_{device} which is against eqn. (8) so that hysteresis will be introduced, as shown in Fig. S8f. If $|C_{FE}|$ is less than C_{eq}, the design satisfies the internal gain condition where SS can be less than 2.3 k_BT/q, as shown in Fig. S8e. When the gate voltage is in subthreshold region, $|C_{FE}|$ is less than C_{eq} among all t_f.

The internal gain condition and non-hysteresis condition are directly related with the C_{fr}. If C_{fr}=0, the internal gain condition ($|C_{FE}|<C_{ox}$) as eqn. (12), can't be fulfilled since the minimum $|C_{FE}|$ obtained for 20 nm HZO from eqn. (2) is about $|C_{FE}|$=13.1 μF/cm^2, which is larger than the C_{ox}=3.54 μF/cm^2 (2 nm Al_2O_3). Therefore, C_{fr} must be considered to fulfill the internal gain conditions, as calculated in Fig. S8e. With the existence of C_{fr}, $|C_{FE}|$ can be smaller than C_{eq}, which fulfills the internal gain condition in eqn. (9). Fig. S8g shows the impact of C_{fr} on the SS vs. I_D characteristics. It is clear that if C_{fr}=0, the SS of the MoS_2 NC-FET is the same as 2.3k_BT/q so that no internal gain can be obtained as predicted by eqns. (12, 13). However, if we consider the impact

of C_{fr}, SS can be less than $2.3k_BT/q$ (internal gain>1) because eqn. (9) is fulfilled as shown in Fig. 8e.

Fig. 8h shows the t_{ox}-t_f design plane of the device. The boundary line between two regions represents the capacitance match: $-C_{FE}=C_{device}$. The cyan area represents the design space of transfer characteristics with non-hysteresis and a steep SS. Even though the subthreshold slope would be reduced when t_f increases, the hysteresis must be avoided in logic applications. Thus, the device geometries (t_f-t_{ox}) should be co-optimized to avoid the hysteresis and achieve a steep SS at the same time.

The simulation results MoS_2 NC-FETs are discussed in details after satisfying the internal gain and non-hysteretic conditions. As shown in Fig. S9a, it can be observed that I_{DS} decreases obviously as t_f increases for a given gate voltage when the device works in the depleted regime ($V_{GS}<V_{FB}$). V_{FB} is defined as the gate voltage when the total gate (or channel) charges reaches zero. In a junctionless transistor, this critical voltage differentiates between depletion-mode subthreshold operation vs. accumulation mode above threshold operation[15]. Note that V_{FB} is bigger than V_{FB0} (flat-band voltage when V_{DS}=0 V) because there is a depleted region in the drain terminal when V_{DS} is not zero. Thus, the increasing of t_f lowers the off-state current significantly and improve threshold voltage compared with its conventional MoS_2 transistor (when t_f=0 nm, a MoS_2 NC-FET is reduced to a MoS_2 transistor). In contrast, in the on-state accumulation regime ($V_{GS}>V_{FB}$), I_{DS} increases when t_f increases. In other words, both on and off state performances improve with t_f, so long the transistor is operated in the NC-FET mode. The phenomenon can be explained as follows. Fig. S9b shows that the interfacial potential (V_{mos}) varying with V_{GS} for different t_f. When V_{GS} is smaller than V_{FB} (in the depleted regime), V_{mos} deceases with t_f increasing while when V_{GS} is bigger than V_{FB} (in the accumulation regime), V_{mos} increase with t_f increasing.

Thus, the off-state current can be lowered and on-state current can be improved at the same time. Among the range of HZO thicknesses possible, t_f=20nm was chosen for processing convenience.

For drift-diffusion based transistors, the subthreshold slope can be estimated as 2.3 $k_BT/(d\varphi_S/dV_{GS})$. For negative capacitance FETs, the DC voltage gain (defined as the body factor $m=d\varphi_S/dV_{GS}$) can be larger than 1, so that SS<2.3 k_BT in this case. Fig. S9c shows that *m* varies with V_{GS} for different t_f. It can be seen that m>1 in the subthreshold regime for a MoS_2 NC-FET and m enlarges when t_f increases for a given V_{GS}. It causes that SS can be smaller 60 mV/dec in a big range of I_{DS} as shown in Fig. S9d. The results from our analytical model match well with those from the experimental data, as shown in Fig. 2.

Fig. S9e shows the transfer characteristics of a MoS_2 NC-FET for different V_{DS}. Contrary to the normal MOSFETs, there is a reverse DIBL effect in the transfer characteristics of the MoS_2 NC-FET. That is, the threshold voltage increases when V_{DS} increases. In order to understand this unique property, the V_{mos} varying with V_{GS} for different V_{DS} is shown in Fig. S9f. One observes that V_{mos} reduces when V_{DS} increases in the subthreshold voltage. On the other hand, V_{DS} has almost no impact on I_{DS} of the intrinsic MoS_2 transistor as shown in Fig. S9g. The reason is that while the DIBL effect of a long-channel intrinsic MoS_2 transistor can be neglected, but this is not true for MoS_2 NC-FET where I_{DS} is reduced with increasing V_{DS}.

The NC-FET also exhibits a characteristic negative differential resistance (NDR) in the output characteristics. Fig. S9h illustrate the output characteristics of a MoS_2 NC-FET for different V_{GS} (with t_f=20 nm). There is a clear NDR effect when the device works in the saturation region ($V_{DS}>V_{GS}-V_{th}$). Simulated V_{mos} vs V_{DS} curves for different V_{GS} are shown in Fig. 3d. It is seen that V_{mos} decreases when V_{DS} increases when the device works in the saturation region. On the other hand, V_{DS} has a small impact on I_{DS} of the intrinsic MoS_2 transistor when the device works in the

saturation region. Thus, V_{mos} dominates the saturation current of the MoS_2 NC-FET. That is, the saturation current is reduced with increasing V_{DS}.

Although the non-hysteretic conditions have been achieved in steady-state, hysteresis during I_D-V_{GS} measurements can still appear as the result of dynamic dumping factor $\rho>0$. Because the steady-state model is ideal while the actual measurement process is dynamic because the rise time of the gate voltage cannot be infinity so that V_{mos} cannot follow the change speed of V_{GS}, which leads to the hysteresis (Fig. S10a). If there is no damping constant, as shown in Fig. S10d and S10e, no hysteresis can be observed for a MoS_2 NC-FET with 20 nm HZO. But if we add a dumping resistor (R_{FE} in Fig. S8b) so that ρ is greater than zero, hysteresis will exist again, as shown in Fig. S10b and S10c. Thus, the second origin of hysteresis is the existence of dumping constant in the ferroelectric HZO.

Based on the discuss above, the hysteresis measured in this work is mostly dumping constant induced hysteresis, as shown in Fig. 2c in manuscript, which is measurement speed dependent. Therefore, our devices fulfill the condition of DC non-hysteretic and internal gain conditions. Meanwhile, by comparing the simulation results on parasitic capacitance, it can be concluded that the damping constant is the origin of the hysteresis and the parasitic capacitance causes the negative DIBL effect, as shown in Fig. S10b-e. And our experimental results in Fig. 3a in the manuscript qualitatively match with simulation results in Fig. S10. The experimental measured dumping factor is $\rho \sim 30\ \Omega$m for ferroelectric HZO[18], which is used in this work for the prediction of working speed for MoS_2 NC-FETs shown in Fig S10f. It can be seen that the MoS_2 NC-FETs still maintain decent hysteresis up to 0.1-1 MHz.

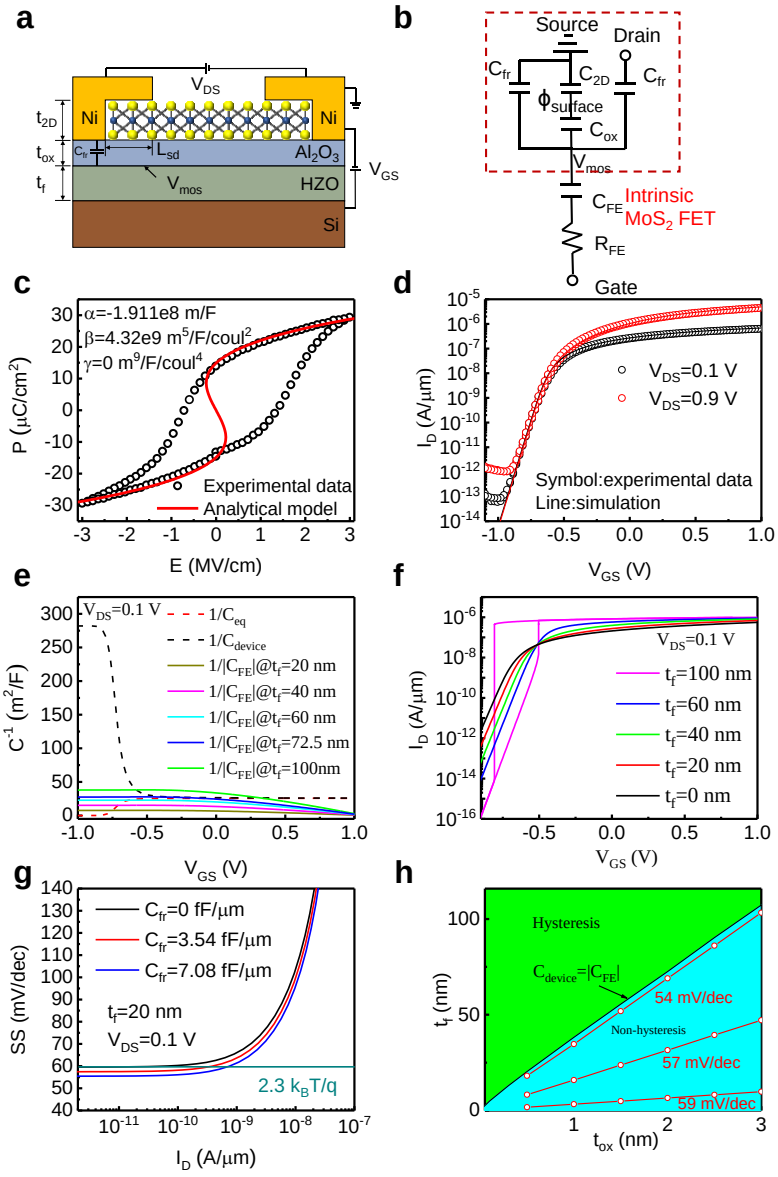

Figure S8 | Experiments and simulations of the internal gain and non-hysteretic conditions on MoS_2 NC-FETs. **a** Cross-section view of the MoS_2 NC-FET in simulation. **b** Simplified small-signal capacitance representation of a MoS_2 NC-FET for steady-state and dynamic simulation. C_{2D} is the capacitance of MoS_2 channel, C_{ox} is the capacitance of the Al_2O_3 layer, and C_{FE} is the capacitance of HZO layer. **c** Experimental polarization-voltage measurement on ferroelectric HZO with MIM structure (TiN/HZO/TiN). **d** I_D-V_{GS} characteristics for MoS_2 NC-FET as in Fig. 2a and the simulation based on parameters extracted from Fig. S8c. **c** Comparison of C^{-1} between C_{eq}, C_{device} and $|C_{FE}|$, which shows $|C_{FE}|>C_{device}$ to fulfill non-hysteretic condition and $|C_{FE}|<C_{eq}$ to fulfill internal gain condition. **d** I_D-V_{GS} characteristics at V_{DS}=0.1 V for HZO films with various thicknesses. $|C_{FE}|<C_{device}$ at 100 nm HZO leads to a large hysteresis in steady-state. **e** SS vs. I_D characteristics at different C_{fr}. **f** The t_{ox}-t_f design plane of the MoS_2 NC-FET. The boundary line represents the capacitance match: $-C_{FE}=C_{device}$.

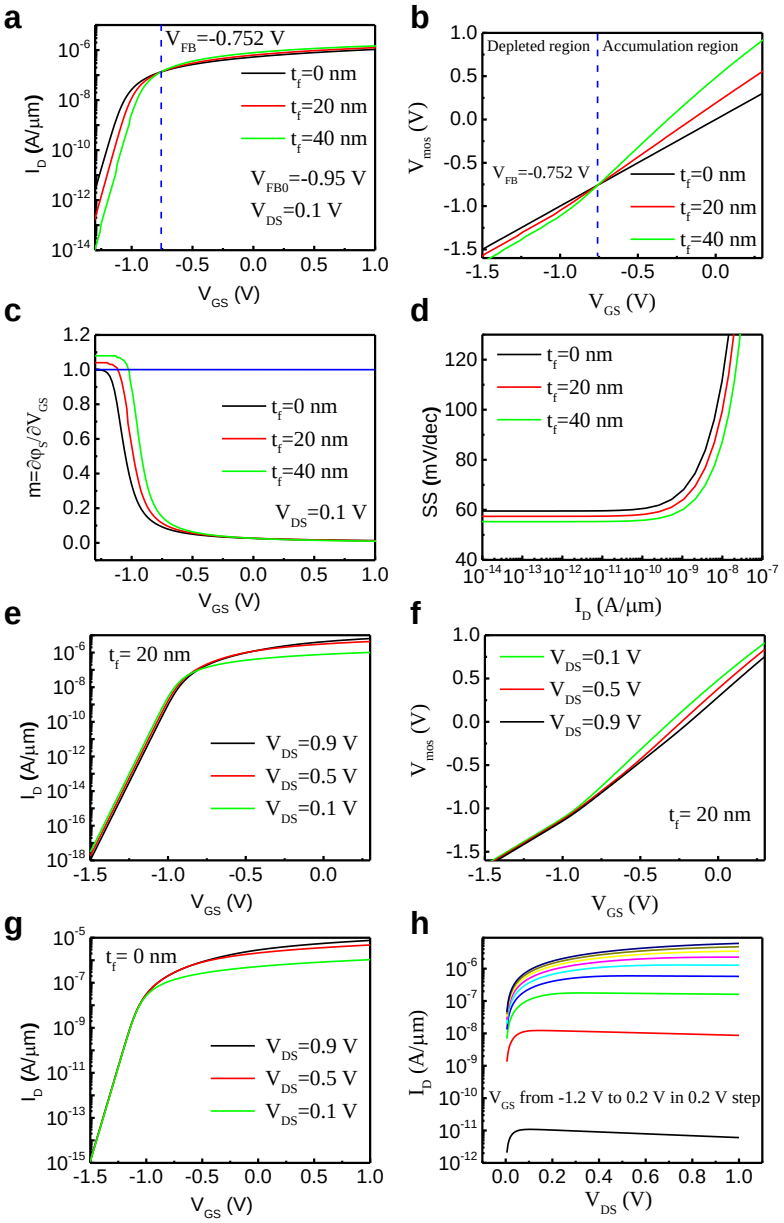

Figure S9 | Simulation of negative DIBL and NDR effect on MoS_2 NC-FETs. a I_D-V_{GS} characteristics of MoS_2 NC-FETs with HZO thickness from 0 nm to 40 nm. **b** Interfacial potential vs. V_{GS} with HZO thickness from 0 nm to 40 nm. **c** DC voltage gain of MoS_2 NC-FETs with HZO thickness from 0 nm to 40 nm. **d** SS-I_D characteristics of MoS_2 NC-FETs with HZO thickness from 0 nm to 40 nm. **e** I_D-V_{GS} characteristics of MoS_2 NC-FETs at different V_{DS}. **f** Interfacial potential vs. V_{GS} of the same MoS_2 NC-FET at different V_{DS}. **g** I_D-V_{GS} characteristics of MoS_2 FETs with no HZO dielectrics at different V_{DS}. **h** I_D-V_{DS} characteristics of MoS_2 NC-FETs at different V_{GS}. Clear NDR can be observed at low V_{GS}.

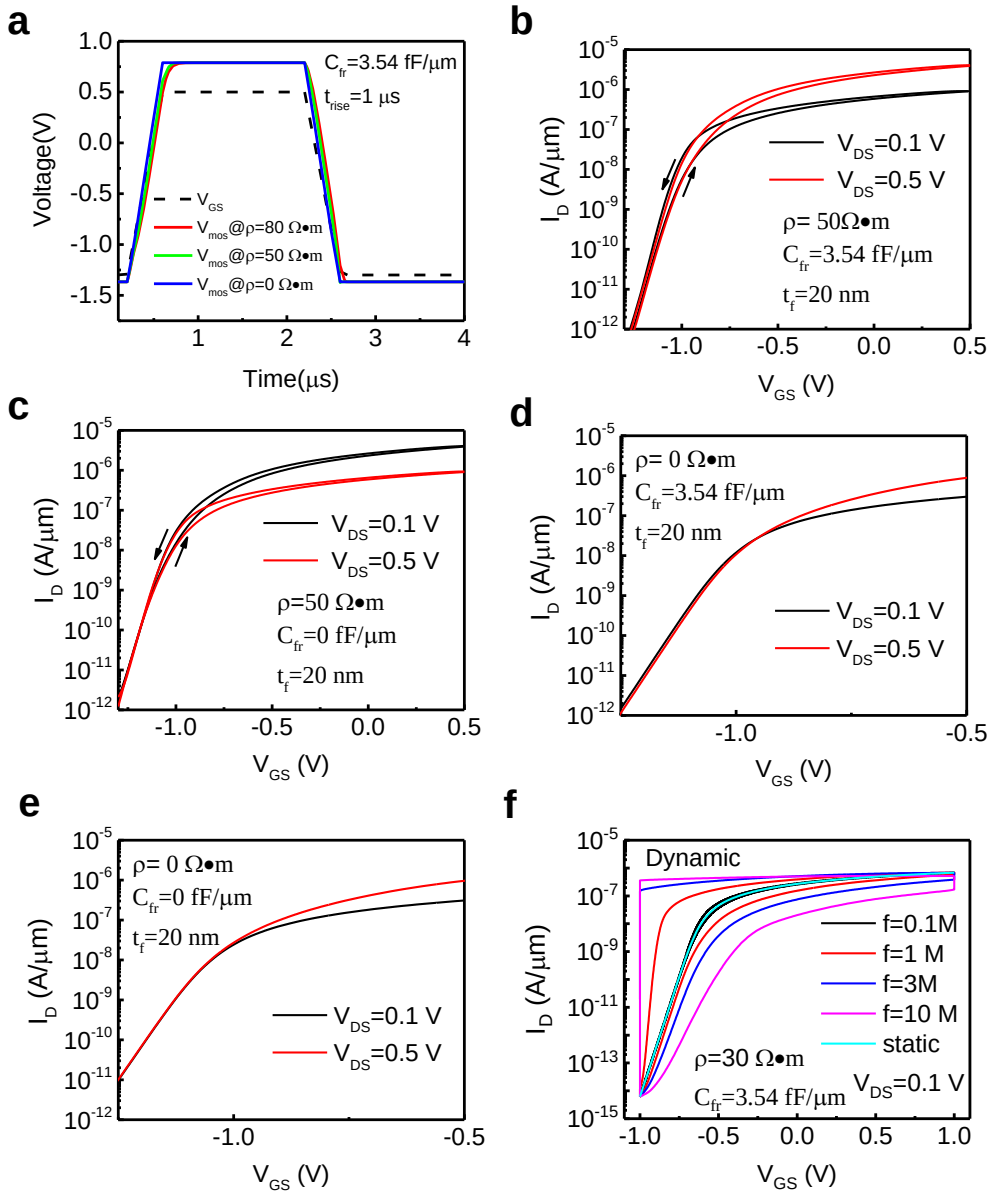

Figure S10 | Simulation on stability and the effects of parasitic capacitance and dumping constant. a Simulated transient behavior of a MoS_2 NC-FET. V_{mos} cannot follow the change of V_{GS}, which leads to the hysteresis. **b** I_D-V_{GS} characteristics with damping constant and parasitic capacitance for different V_{DS}. **c** I_D-V_{GS} characteristics with damping constant and without the parasitic capacitance for different V_{DS}. **d** I_D-V_{GS} characteristics without damping constant and with the parasitic capacitance for different V_{DS}. **e** I_D-V_{GS} characteristics without damping constant and without the parasitic capacitance for different V_{DS}. **f** I_D-V_{GS} characteristics for a MoS_2 NC-FET at different frequencies.

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